

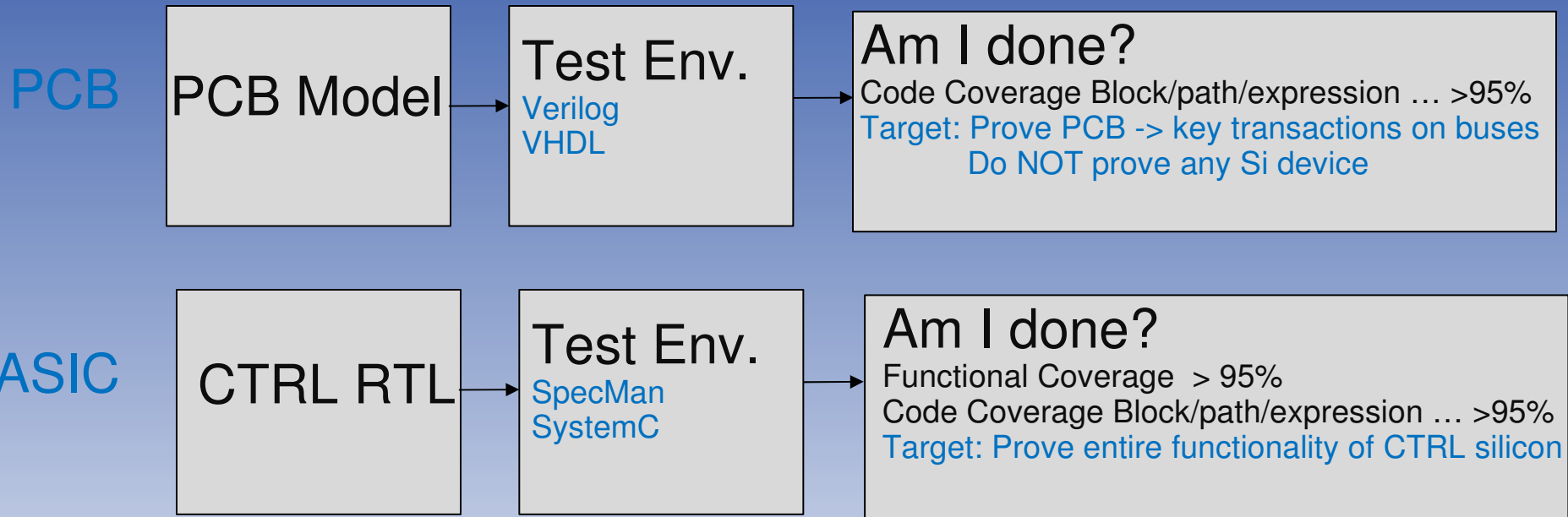


Tailoring Verification Models to Customer Needs

Stephan Rosner – Spansion, LLC

Richard Munden – Free Model Foundry

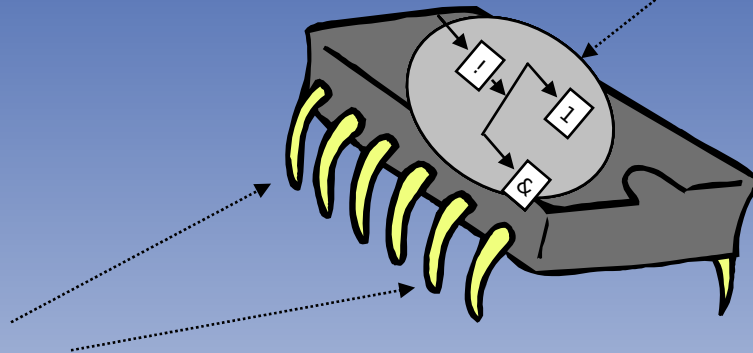
Two Types of Verification Activities



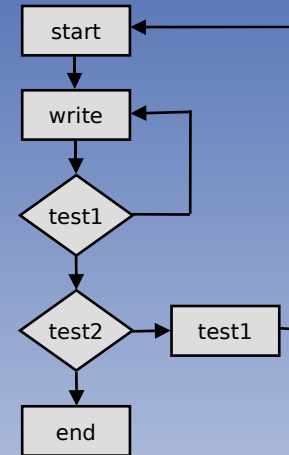
- ASIC and PCB verification have different focus

What Models are Needed for Board-Level Verification?

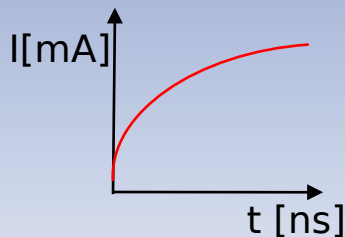
Verilog/VHDL/C:



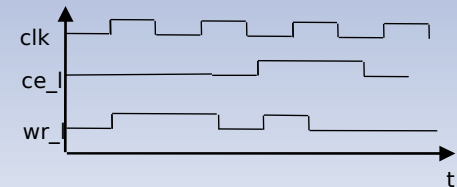
behavioral



IBIS: I/O characteristics for circuit simulation

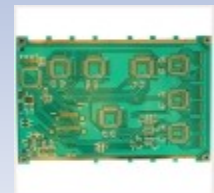
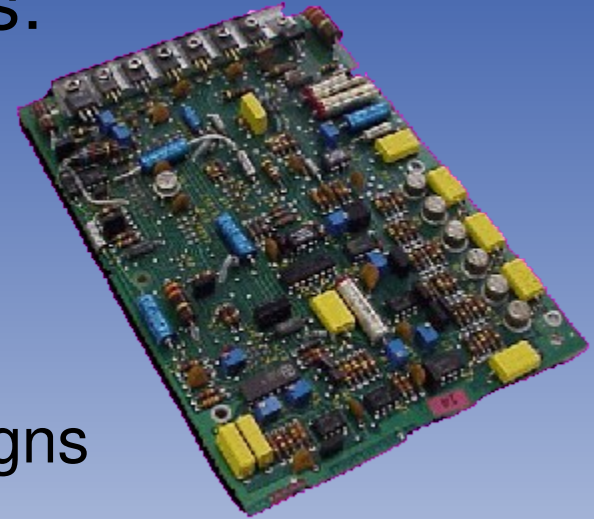


timing



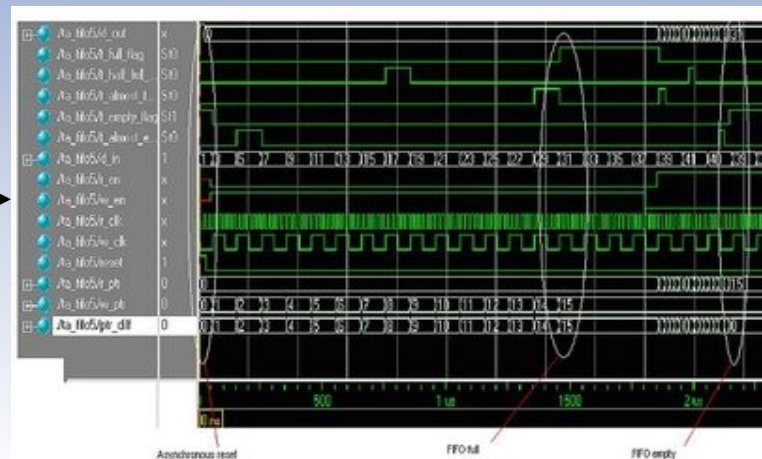
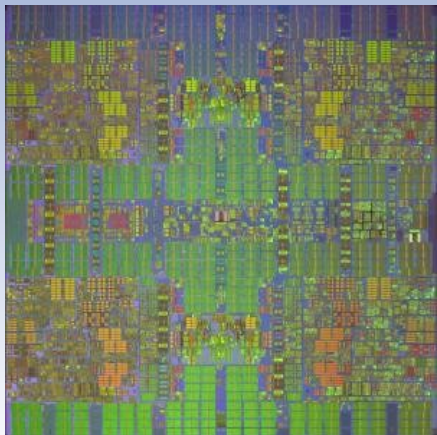
Board-Level Verification

- Board designers face problems:
 - Interconnects
 - Development time
 - Board spins
- This is FMF's world
 - Used in thousands of board designs
 - Saved time and money
 - Accelerate customers time to volume purchase

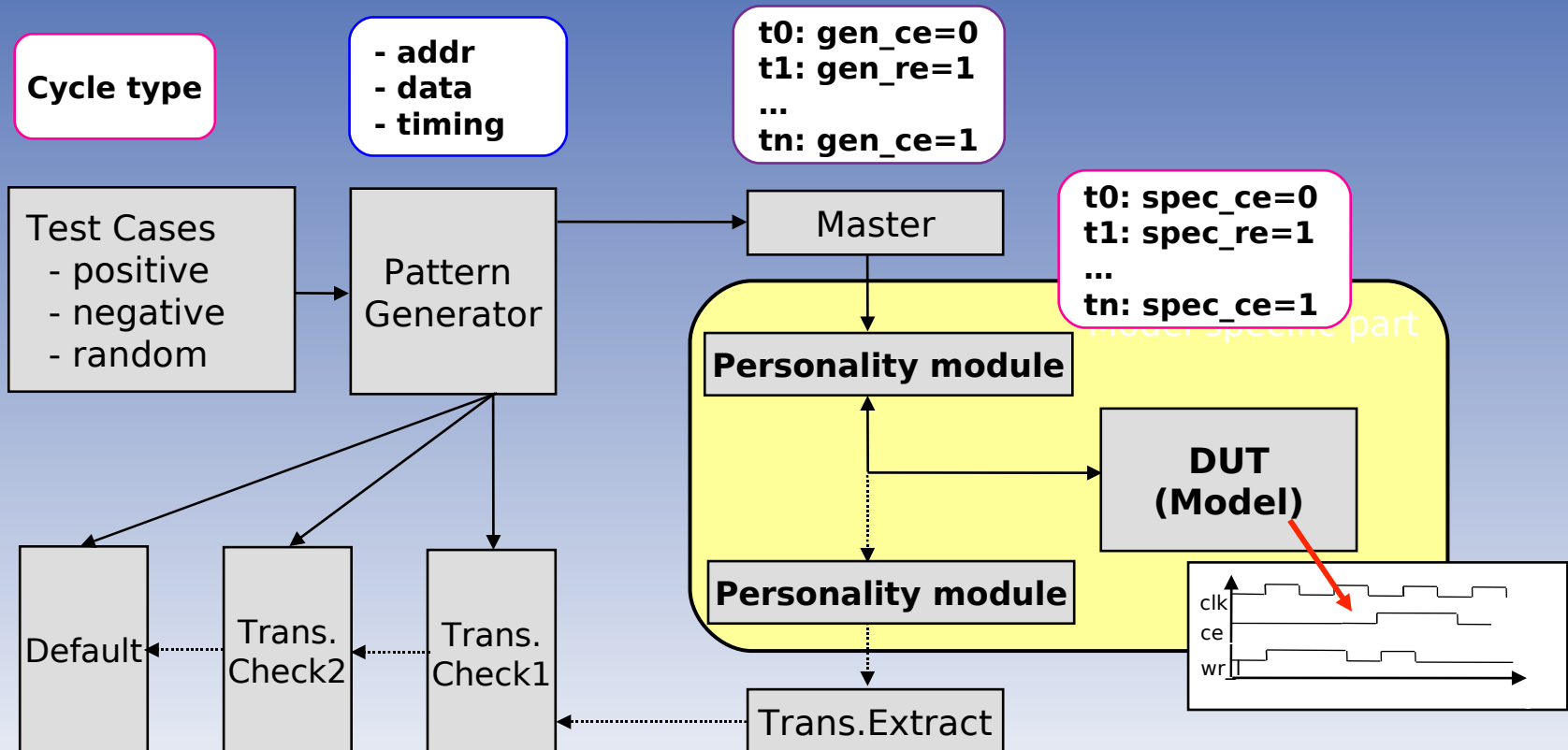


Chip-Level Verification

- ASIC designers face problems:
 - IP integration
 - Endless verification
- This is Denali's world
 - Few, but very expensive projects
 - Expensive, specialized verification tools
 - Dedicated verification engineers



Reliable Models and Superior Support - FMF verification Flow



Reliable Models and Superior Support - FMF Issue Tracking

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| 168 | s29xdx512s.v & s29xdx512s.vhd Burst Read munden@modelfoundryservices.com | new 2 months ago | bugs 2 months ago | b-bizic | 20 0 |
| 169 | VITAL timing generics - IF library munden@modelfoundryservices.com | new 2 months ago | bugs 2 months ago | b-bizic | 20 0 |
| 170 | Im75 compiler warnings munden@modelfoundryservices.com | new 2 months ago | bugs 2 months ago | b-bizic | 20 0 |
| 172 | S29j032h0 simulation Issue munden@modelfoundryservices.com | new 3 weeks ago | bugs 3 weeks ago | b-bizic | 20 0 |
| 173 | Verilog model issues - June 25 - vital-FMF-s29xds02gs-2008-05-06-1.tar.gz roni.kornitz@spansion.com | new 2 weeks ago | bugs 2 weeks ago | kornitz | 20 0 |
| 174 | XDS-R models - burst read behavior roni.kornitz@spansion.com | new 11 days ago | bugs 11 days ago | kornitz | 20 0 |

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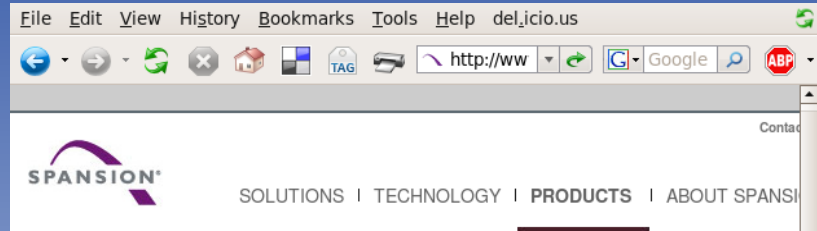
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Reliable Models and Superior Support - FMF Model Availability

| Part | Distributor | Qty | Date |
|----------------|-------------------------|-----|------------|
| 70T3519S133BFI | NU HORIZONS ELECTRONICS | 1 | 07/13/2008 |
| 70T3519S166BCI | AVNET | 2 | 07/13/2008 |
| 70T3519S200BC | AVNET | 6 | 07/13/2008 |

| Type | Title | Size | Revision Date |
|-----------------------|---|--------|---------------|
| Application Note | AN-144, Sync Dual-Ports for DSP & Communication Applications | 103 KB | 05/30/2006 |
| | AN-253, Introduction to Multi-Port Memories | 36 KB | 05/30/2006 |
| | AN-254, The Most Commonly Asked Questions About Sync Dual-Ports | 66 KB | 05/30/2006 |
| | AN-255 Dual-Port Power Discussion | | |
| Datasheet | AN-09, Dual-Port SRAMs Yield Bit-Slice Design | | |
| | AN-409 DP Memory Simplifies Wireless BaseS | | |
| | AN-68, Dual-Port SRAM Simplifies PC-to-TMS | | |
| Model - BSDL | 70T3519 BSDL Model | | |
| Model - IBIS | 70T3519 IBIS Model | | |
| Model - VHDL | 70T3519 VHDL Model | | |
| Model - Verilog | IDT70T3519 Verilog Model | | |
| Product Change Notice | PCN#A-0305-02, new m/c G770 & 2300 d/a m | | |



- ### PRODUCTS
- MirrorBit® NOR
 - MirrorBit® ORNAND™
 - MirrorBit® HD-SIM

Simulation Modeling and CAD Modeling Support

There are several categories of simulation models and CAD models available for Spansion® Flash memory devices:

- For digital circuit simulation and timing verification, the most common model formats are VHDL and Verilog. They replicate command inputs and outputs as found in the device datasheet.
- For signal integrity tests and transition response, the preferred model is IBIS format.

Free Model Foundry
Open Source Simulation Models for System Level Verification

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Search Models

FMF VHDL Models

All the FMF models are VHDL 93 and VITAL2000 compliant and require the VITAL2000 library for correct compilation. They are designed for timing backannotation by means of an SDF file. The intrinsic delays default to 1 ns. We have a tool to read internal delays from an external file (in XML) and add them to the simulation through a SDF file. The most recent version is written in perl and may be downloaded from the "FMF Tools" area. Timing files are provided for over 11,000 part numbers.

Also in the tools area is the document type definition (dtd) for the timing files. FMF MAKES NO WARRANTIES ON THE PERFORMANCE OF ANY MODELS IN ITS DATA REPOSITORY. USERS ARE RESPONSIBLE FOR VERIFYING THE ACCURACY OF THE MODELS, SOFTWARE OR TOOLS PROVIDED (TEST SUITES, PACKAGES, TIMING, ETC.).

How models are copyrighted

Model List updated 2008 July 13

Individual models and timing files, may not be accessed directly from this page. Only entire libraries can be downloaded using the library links below. To download individual file or to view data sheets, use the Model List link above. Data sheets describe the models and what part numbers are covered in the timing files.

FMF Tools

A new version of mk_sdf was added to the tools directory 2007 October 14. This version supports the use of wrappers in CAE libraries.

FMF Packages (required for the models)

Version 2.5 of the flip-flop package (ft_package.vhd) was released on 2007 July 01. This release addresses issue with the DREG and DREGGN tables.

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Learning By Example-VHDL
Get up & running quickly. Over 60 worked examples on an FPGA Board!
www.itebooks.com

VHDL Test Benches
Generate VHDL models from timing diagrams or logic analyzer data.
www.syn cad.com

Common Data Model
Provide a Common Data Model for SOA-Based Applications.
www.progress.com/dataxtend

Verilog
Effective Verification Platform w/ Ease of Use & Visibility of RTL
www.Eve-Team.com

Healthy Heart Secrets
3 Free Guides! Natural Remedies for Cholesterol, Blood Pressure, Clots.
DiscoverTrueHealth.com

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Santa Clara, CA USA
August 2008

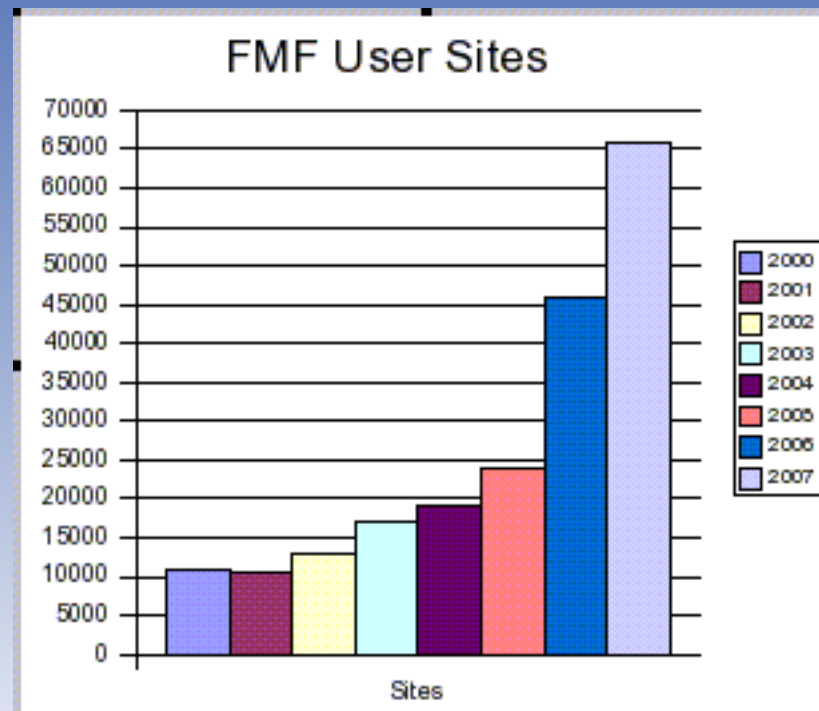
A Typical Use Case for FMF Models

- System Verification
 - Flash Interfaces with FPGAs and Std Components
 - Uses “standard” VHDL and Verilog tools
 - Models of non-memory components also required
 - Little or no budget for models
 - Good fit for free, open source models



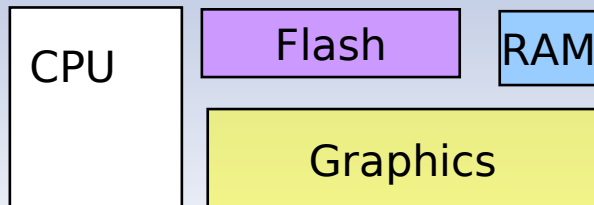
Industry Proven FMF Models

The number of sites using FMF models continues to grow



Key Features of Foundry Models

- Models are open source VHDL and Verilog
 - Engineers can read and understand models
 - Models can be archived and used as long as needed
- Models are Optimized for Board-Level Verification
 - Allow backannotation of interconnect delays
 - Integrate well with schematic capture tools



| |
|---|
| // Global SDF file |
| // SDF RAM - not available |
| // SDFGraphics (IOPATH A0 DQ0 (30:60:90) (30:60:90)) |
| ... |
| // Flash SDF (IOPATH RDY WR (30:60:90) (30:60:90)) |
| ... |
| // SDF CPU - not available |

Free Model Foundry Models

- Written At Highest Level of Abstraction Practical
 - Very fast simulation
 - Can be created from datasheets only
 - Non-synthesizable
- Paid for by Manufacturer
 - Free to all potential customers
 - No barrier to trial
 - Accelerate customers time to volume purchase

Spanansion Success Story

- Spanansion uses FMF models for its complete portfolio
 - In 2007, monthly downloads of Spanansion models exceeded 40,000
 - These downloads are from the FMF website only
 - Spanansion website downloads are not monitored.
 - Download numbers continue to increase
 - Spanansion funds models so its customers do not have to

Conclusions

- FMF Provides Open Source Models
 - Models are free to end users
- Models are Very Popular among Designers
 - More than 810,000 downloads in 2007
 - Over 200 companies and Universities are registered with FMF
 - Registration is not required for downloading
- Models Solve Critical Problem of PCB Verification

Your Chip Doesn't Work in a Vacuum

